15nm Gate Length Planar CMOS Transistor

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Abstract

Continued scaling of mainstream planar CMOS transistor technology into the deep-sub-100nm regime is increasingly challenging but possible. In this paper, we report bulk-silicon planar CMOS transistors with the physical gate length scaled down to 15nm. Gate delays (CV/I) of 0.29ps for n-channel FET and 0.68ps for p-channel FET are achieved at a supply voltage of 0.8V. Energy-delay products are 42pJ-ps/m for n-channel FET and 97pJ-ps/m for p-channel FET, respectively. To our knowledge, these numbers are the best reported to date.

Introduction

The 2001 ITRS roadmap declares the continual scaling of CMOS for five more generations in the sub-100nm regime. CMOS scaling is at a critical juncture, forcing differences from the classic physical scaling methodology used to date. Approaching the fundamental limits of transistor drives the industry and research community to actively search for alternative materials and new device architectures.

The great momentum of IC industry, however, will push the existing planar CMOS technology down to its physical limit. Significant device design and process barriers must be overcome in order for transistors to meet the ITRS targets. In this late-news paper, we report aggressively scaled planar CMOS transistors, with discussion on the major fabrication challenges, device scalability and performance.

Design & Fabrication

Physical Gate Length Scaling

The new ITRS roadmap specifies more aggressive L_g scaling than the last version. Industry tends to outpace the roadmap, especially for high-performance products (Fig.1). Lithography will advance from 248nm to 193nm or 157nm in the near future. Fig.2 illustrates a MOS transistor with a gate length of 15nm, patterned by 248nm DUV lithography. Fig.3 and 4 show the MOS transistor's I-V electrical characteristics. The drive currents of 615μA/μm (n-FET) and 265μA/μm (p-FET) are measured at V_{dd}=0.8V, with I_{off} <500nA/μm for both devices. The transistors are the smallest planar CMOS devices reported to date. For transistors with such small L_g, control of gate line edge roughness (LER) is very important. Device off-state leakage current increases due to large LER and makes transistor design more difficult.

Gate Dielectrics Scaling

High-k dielectric and metal gate will be needed to meet the 6Å EOT (11Å inversion CET) target for 15nm CMOS according to ITRS 2001 roadmap (Fig.5). In this experiment, poly-Si gate and 8Å EOT (14Å physical) nitride/oxynitride (N/O) stack were used as the gate stack; see Fig.6. Rapid oxygen diffusion into the gate edge during poly-Si sidewall oxidation results in excessive gate edge oxidation in such a small device (Fig.1). Aggressive EOT scaling of the N/O gate dielectric stack is limited by increased tunneling leakage and channel mobility degradation.

Ultra-Shallow Junction

Ultra-shallow and highly activated source/drain extension is vital to control the short-channel effects. Traditional RTA is limited by dopant solid-solubility. By using amorphization implant along with low-Dt process, lower sheet resistance is attained for shallower junction. Further reduction of X_j-R_{sh} would possibly need non-conventional technique such as laser anneal that has "zero" Dt and super-activation feature [18]

Channel Design

Channel profile design to control short-channel effect is extremely important in sub-20nm planar transistors. The advantages of steep retrograde wells diminish CMOS as L_g shrinks. Reduced Dt is needed to make a highly compact and ultra-shallow halo profile. Less dopant activation in the junctions due to reduced Dt is among the challenges.

Salicide

NiSi is used due to its better scalability for sub-50nm CMOS [7]. NiSi also allows low-thermal budget in the fabrication process, minimizing the dopant diffusion and deactivation in poly-Si gate and source/drain junctions.

Performance & Scalability

Both vertical and lateral electric fields increase as a result of aggressive CMOS dimensional scaling (Figs 7-8). The drive current per unit gate capacitance increases largely due to the relaxation of I_{off} tolerance for deeply scaled devices (Fig.9). In the new ITRS roadmap, the transistor I_{on} target is lifted as a result of relaxed I_{off} spec to ensure sufficient gate over-drive. The maturity of critical process elements such as gate stack with ultra-thin CET and ultra-shallow highly activated junctions is critical in order to achieve the performance goal as well as to control the short-channel effects.

Significant reduction of gate delay (CV/I) and energy-delay product results from the aggressive transistor scaling. The 15nm CMOS devices exhibit gate delays of 0.29ps for n-channel FET and 0.68ps for p-channel FET at a supply voltage of 0.8V (Fig.10). Energy-delay products are 42pJ-ps/m for n-FET and 97pJ-ps/m for p-FET, respectively (Fig.11).

Summary

We have demonstrated planar CMOS with a physical gate length of 15nm. Record gate delay and energy-delay product were achieved. Continued efforts on critical elements such as high-k gate dielectric, metal gate electrode and ultra-shallow junction will drive planar CMOS, as a mainstream technology for high-performance ICs, to its physical scaling limit.

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Capacitor Test Structures for C-V Measurements on CMOS Devices with Sub-20 Å Oxides

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CITING DOCUMENTS

1. Optimization of Gate Leakage and NBTI for Plasma Nitrided Gate Oxides by Numerical and Analytical Models Islam, A.E.; Gusta, G.; Ahmad, K.Z.; Maheshwari, S.; Alam, M.A.
Electron Devices, IEEE Transactions on
On page(s): 1143 - 1152 , Volume: 56 Issue: 5 , May 2009 Abstract | Full Text: PDF (969KB)

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Sub-100 nm nMOSFETs with direct tunneling thermal, nitrous and nitric oxides

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ABSTRACT

Performance and reliability of sub-100 nm gate length devices using a dual gate and shallow trench isolated CMOS technology were investigated. Ultra-thin direct tunneling (DT) thermal, nitrous and nitric oxides as thin as 1.3 nm are used. Only N-MOS device results are reported here. The ultra thin DT gate oxides are produced by a furnace oxidation with a dilute oxygen flow. Nitrous and nitric oxides are formed respectively by N_2O and NO treatments. The sub-100 nm gate length is realized by a resist trimming technique combined with deep ultra-violet lithography. For the 90 nm gate length (CD SEM) MOSFET with 2.2 nm physical thickness (TEM) of nitrous oxide on the source/drain (S/D) area produced here, the poly profile is almost vertical and the poly gate etch has high selectivity to avoid S/D gate oxide pitting, even with oxide thickness down to 1.3 nm.

INDEX TERMS

- **INSPEC**

Controlled Indexing

MOSFET , dielectric thin films , etching , isolation technology , nanotechnology , nitridation , oxidation , semiconductor device reliability , semiconductor device testing , tunneling , ultraviolet lithography

Non Controlled Indexing

1.3 nm , 100 nm , 2.2 nm , 90 nm , CD SEM , MOSFET , N-MOS device , N_2O , N_2O treatment , NO , NO treatment , O_2 , S/D gate oxide pitting , Si , SiO_2 , Si-SiON-Si , TEM , deep ultraviolet lithography , dilute oxygen flow , direct tunneling nitric oxide , direct tunneling nitrous oxide , direct tunneling thermal oxide , dual gate shallow trench isolated CMOS technology , furnace oxidation , gate length , nMOSFETs , nitric oxide , nitrous oxide , oxide physical thickness , oxide thickness , poly gate etch selectivity , poly profile , reliability , resist trimming technique , source-drain area , ultra thin DT gate oxides

CITING DOCUMENTS

1. Hot carrier degradation of HfSiON gate dielectrics with TiN electrode , Shin, J.H. , Byoung Hun Lee , Rino Choi , Seung Chul Song , Bernstein, K. , *Device and Materials Reliability, IEEE Transactions on*
On page(s): 177 - 182 , Volume: 5 Issue: 2 , June 2005
Abstract | Full Text: PDF (560KB)
2. Impact of tunnel currents and channel resistance on the characterization of channel inversion layer charge and polysilicon gate depletion of sub-20 Å gate oxide MOSFETs , Ahmed, K. , Ibok, E. , Yeap, G.C.F. , Qi Xiang , Ogle, B. , Wortman, J.J. , Hauser, J.R. , *Electron Devices, IEEE Transactions on*
On page(s): 1650 - 1655 , Volume: 46 Issue: 8 , Aug 1999
Abstract | Full Text: PDF (212KB)
3. A comparative study of gate direct tunneling and drain leakage currents in n-MOSFET s with sub-2 nm gate oxides , Yang, N. , Henson, W.K. , Wortman, J.J. , *Electron Devices, IEEE Transactions on*
On page(s): 1636 - 1644 , Volume: 47 Issue: 8 , Aug 2000
Abstract | Full Text: PDF (236KB)
4. Projecting lifetime of deep submicron MOSFETs , Ershun Li , Rosenbaum, E. , Jiang Tao , Peng Fang , *Electron Devices, IEEE Transactions on*
On page(s): 671 - 678 , Volume: 48 Issue: 4 , Apr 2001
Abstract | Full Text: PDF (196KB)